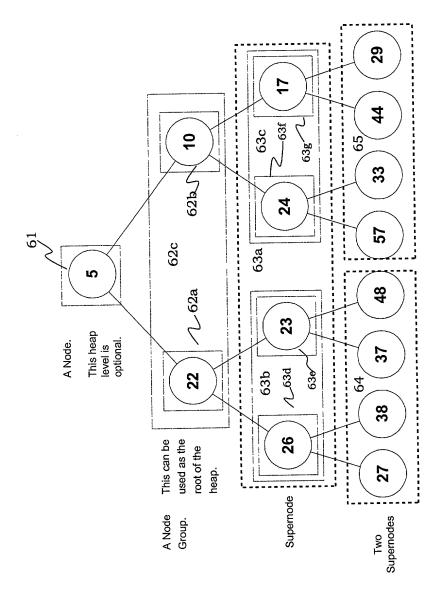


FIGURE 5



## FIGURE 6

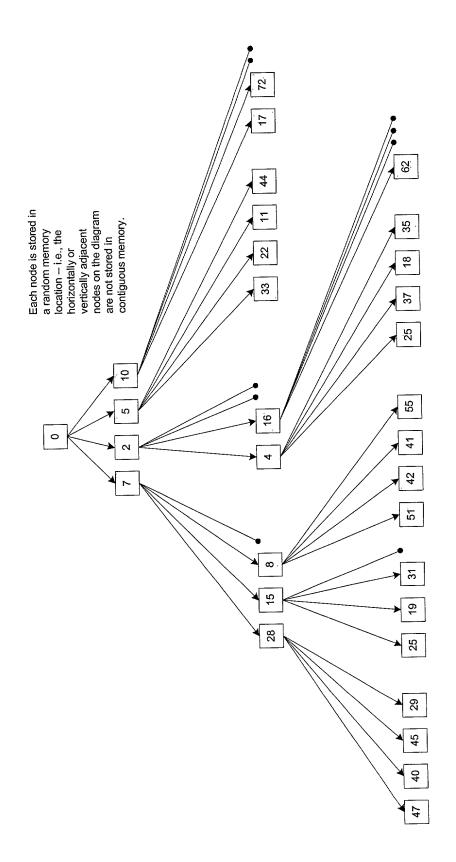


FIGURE 7

<u>70</u>

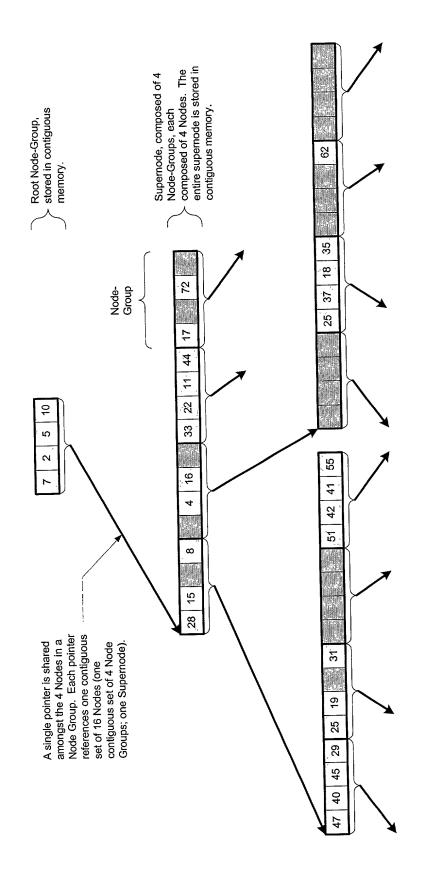
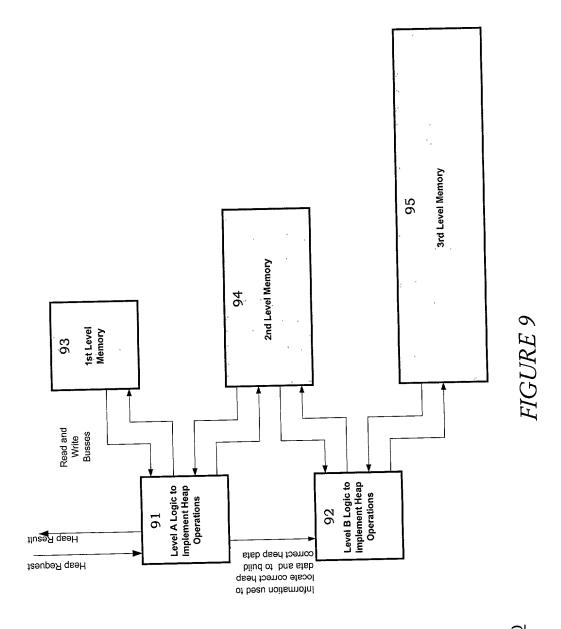
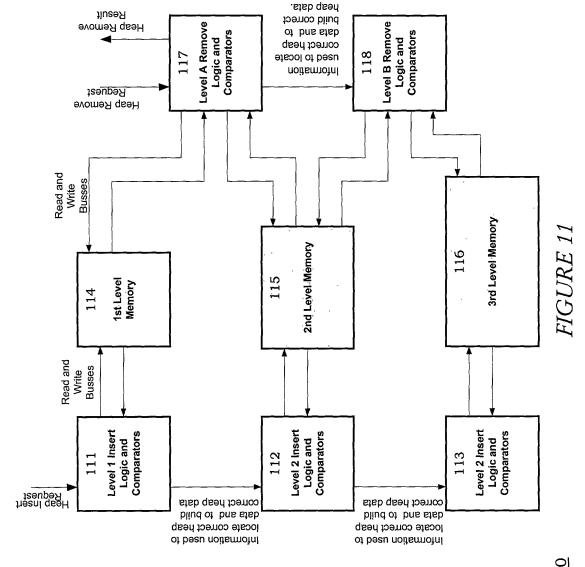


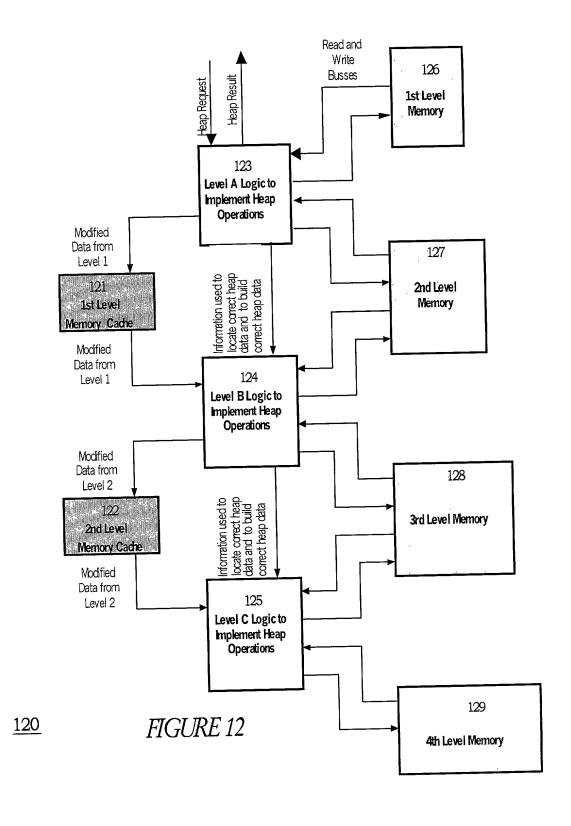
FIGURE 8



	time> 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Read Level 1 RAM	Α						В					_			_			_
Write Level 1 RAM						Α						В						
Level A Comparisons				Α	Α				<u> </u>	В	В							<u> </u>
Read Level 2 RAM			Α			L			В							ļ		<u> </u>
Write Level 2 RAM								Α	<u> </u>			_		В				<u> </u>
Level B Comparisons						Α	Α				_	В	В				_	<del> </del>
Read Level 3 RAM					Α						В		<u> </u>		ļ	<u> </u>	-	
Write Level 3 RAM										Α	<u> </u>	<u> </u>	<u> </u>		<u> </u>	В	<u> </u>	<b>├</b> ─
Level C Comparisons						<u> </u>		Α	Α			_	1	В	В	<u> </u>	<u> </u>	ـــ
Read Level 4 RAM							Α	<u> </u>	<u> </u>		<u> </u>		В	<u> </u>	ļ	_	-	↓_
Write Level 4 RAM						1_	<u> </u>			Α		<u> </u>				В	<u> </u>	<u></u>

FIG. 10





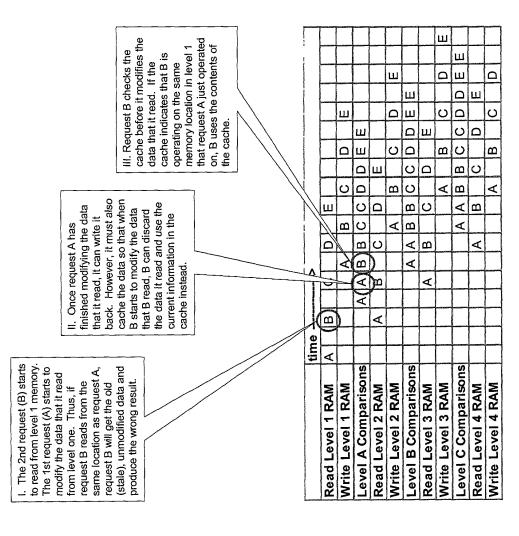


FIGURE 13

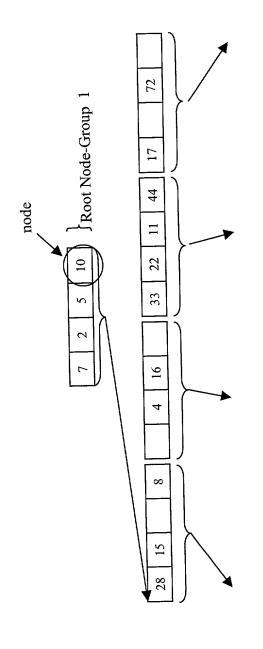
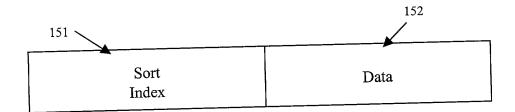


FIG. 14



<u>150</u>

FIG. 15

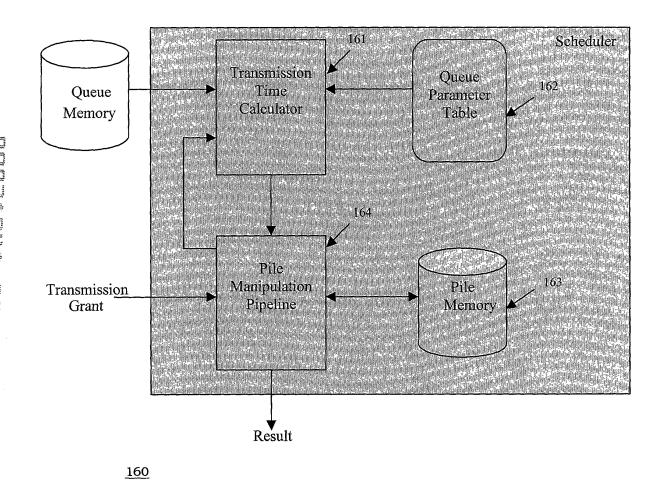
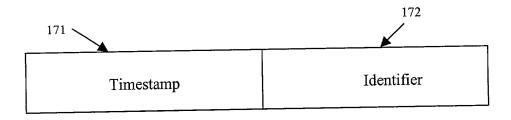
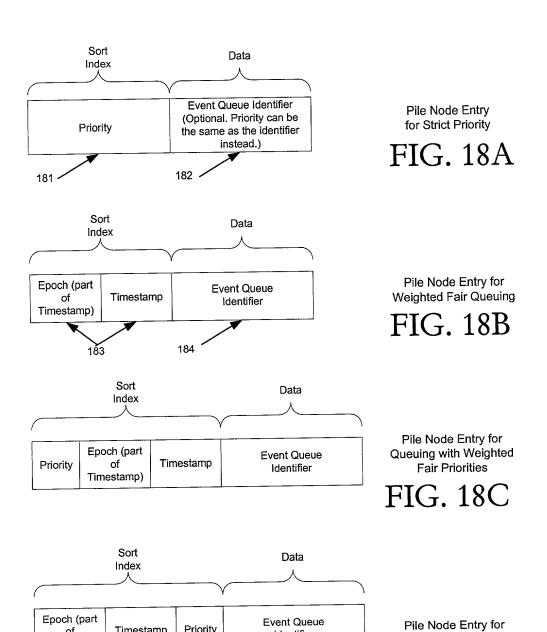


FIG. 16



<u>170</u>

FIG. 17



Identifier

187

Traffic Shapping

FIG. 18D

Priority

Timestamp

186

of

Timestamp)

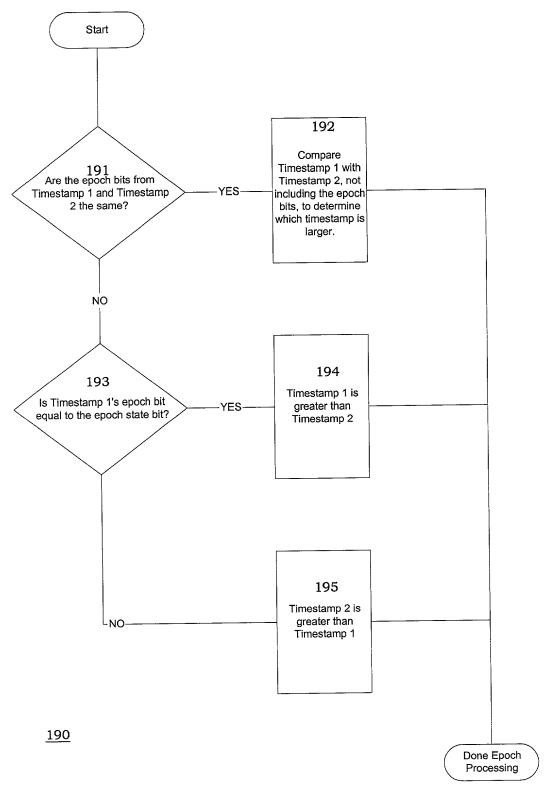
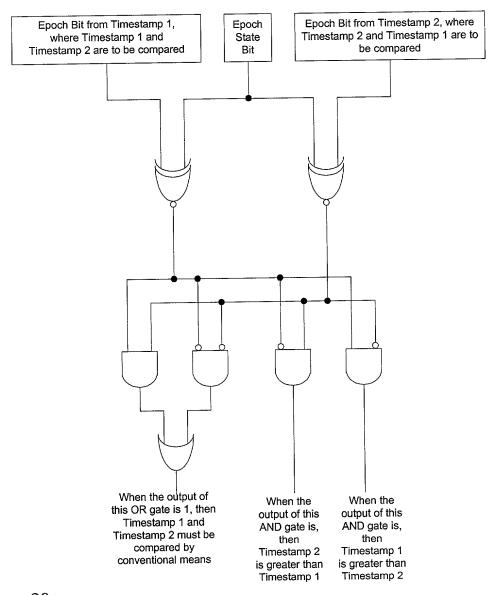
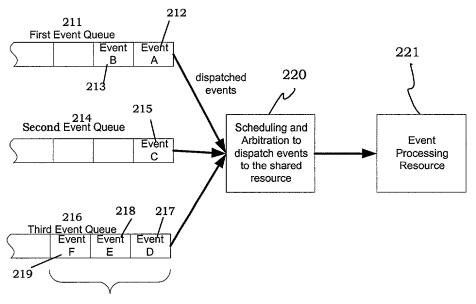


FIG. 19



<u>20</u>

FIG. 20



Events D, E, and F must be dispatched in order. However, Events D, C, and A are dispatched in an order determined by the Scheduling and Arbitration block.

## FIGURE. 21